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Description

METHOD FOR CONTROLLING CRITICAL DIMENSION BY UTILIZING RESIST SIDEWALL PROTECTION

BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to semiconductor fabrication processes. More particularly, the present invention relates to a critical dimension (CD) control method for semiconductor fabrication processes. According to the present invention method, one skill in the art is capable of making a nano-scale gate structure with an After-Etch-Inspection CD (AEI CD) that is substantially equal to After-Develop-Inspection CD (ADI CD) thereof.

[0003] 2. Description of the Prior Art

[0004] n the fabrication of semiconductor devices, it is typical to use photoresist layer on a semiconductor wafer to mask a predetermined pattern for subsequent etching or ion im-

plantation processes. The patterned photoresist is usually formed by, firstly, coating the photoresist, exposing it to suitable radiation (UV, EUV, e-beam, etc.), and then developing (and baking) the exposed photoresist. For positive-type photoresist, for example, the irradiated parts of the photoresist are chemically removed in the development step to expose areas of the underlying layer where are to be etched. As known in the art, quality inspections are carried out after development and after etching, respectively, to ensure good quality of the device critical dimensions (CDs), which are also referred to as After-Develop-Inspection CD (ADI CD) and After-Etch-Inspection CD (AEI CD). These quality control procedures are designed to remedy any process anomaly in time.

[0005] As the feature size of the semiconductor devices shrinks, the difference between the ADI CD and AEI CD becomes larger. This turns out to be a serious problem when the device dimension shrinks to nano scale and beyond. Referring to Fig.1 and Fig.2, the prior art processes for defining a sub-micro or nano-scale gate structure as an example are schematically demonstrated. On a main surface of a semiconductor substrate 10, a gate dielectric layer 12, a polysilicon layer 14, a tungsten silicide layer

16, and a silicon nitride cap layer 18 are sequentially deposited to constitute a stacked structure 20. A photoresist layer (not explicitly shown) is coated on the top of the stacked structure 20. The photoresist layer is subjected to conventional lithography to transfer a gate pattern on a photo mask to the photoresist layer. In Fig.1, the gate pattern transferred to the photoresist is denoted with numeral 30 and has an ADI CD of W_1. Using the photoresist (PR) gate pattern 30 as an etching mask, according to the prior art, an anisotropic dry etching is performed to etch away the non-masked silicon nitride cap layer 18, thereby transferring the gate pattern 30 to the silicon nitride cap layer 18. Thereafter, using the patterned silicon nitride cap layer 18 as an etching hard mask, the dry etching continues to etch the exposed tungsten silicide layer 16 and the polysilicon layer 14, thereby forming a gate structure 40, as shown in Fig.2. The resultant gate structure 40 has an AEI CD of W_2. In most cases, it is desired to have an ADI CD (W_1) that is substantially equal to the AEI CD (W_2), because it directly affects the channel length of a transistor device. However, in practice, the AEI CD (W_2) is significantly smaller than ADI CD (W_1).

[0006] One approach to solving the above-mentioned problem is

increasing the ADI CD of the gate pattern 30 for compensating the CD loss during the subsequent dry etching. Unfortunately, this prior art method is difficult to control and is not cost-effective. Consequently, there is a constant need in this industry to provide a method for improving nano-scale gate fabrication such that the ADI CD (W_1) is substantially equal to the AEI CD (W_2).

Summary of Invention

[0007] It is therefore the primary object of the present invention to provide a method for controlling critical dimensions in the fabrication of semiconductor features. According to the present invention, a reliable and effective method is provided for making a nano-scale gate structure with an After-Etch-Inspection CD (AEI CD) that is substantially equal to After-Develop-Inspection CD (ADI CD) thereof.

[0008] In accordance with the claimed invention, a critical dimension (CD) control method for semiconductor fabrication processes is provided. A silicon or semiconductor substrate is provided. A semiconductor layer such as a polysilicon layer is deposited on the substrate. A cap layer is then deposited on the semiconductor layer. A photoresist pattern is formed on the cap layer by lithography. The photoresist pattern has a top surface and vertical side-

walls. A silicon thin film is selectively sputterred on the top surface and vertical sidewalls of the photoresist pattern, but substantially not on the cap layer. Using the silicon thin film and the photoresist pattern as etching hard mask, an anisotropic dry etching is carried out to etch the cap layer, thereby transferring the photoresist pattern to the cap layer. The anisotropic dry etching continues, using said patterned cap layer as etching hard mask to etch the semiconductor layer. According to the claimed invention, thickness of the silicon thin film on the vertical sidewalls is "x", while thickness of the silicon thin film on the top surface is "y", wherein xx<, preferably, xx<0 angstroms.

[0009] Other objects, advantages and novel features of the invention will become more clearly and readily apparent from the following detailed description when taken in conjunction with the accompanying drawings.

Brief Description of Drawings

[0010] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. In the drawings:Fig.1 and Fig.2 demon-

strate the prior art processes for defining a sub-micro or nano-scale gate structure in cross-sectional views; and- Fig.3 to Fig.6 are schematic cross-sectional diagrams showing the method for controlling critical dimensions by utilizing photoresist sidewall protection according to one preferred embodiment of the present invention.

DETAILED DESCRIPTION

[0011] Please refer to Fig.3 to Fig.6. Fig.3 to Fig.6 are schematic cross-sectional diagrams showing the method for controlling critical dimensions in the fabrication of a nano-scale gate structure according to one preferred embodiment of the present invention. It is to be understood that the embodiment illustrated through Fig.3 to Fig.6 is only exemplary. Those skilled in the art should know that the present invention could be applied in making other semiconductor features in the fabrication of integrated circuits, for example, definition of contact holes, for improving variation between ADI CD and AEI CD. As shown in Fig.3, a semiconductor substrate 10 is provided. A gate dielectric layer 12, a polysilicon layer 14, a tungsten silicide layer 16, and a silicon nitride cap layer 18 are sequentially deposited on a main surface of the semiconductor substrate 10 to form a stacked structure 20. A photoresist layer (not

explicitly shown) is coated on the top of the stacked structure 20. The photoresist layer is subjected to conventional lithography to transfer a gate pattern on a photo mask to the photoresist layer. In Fig.3, the gate pattern transferred to the photoresist is denoted with numeral 30 and has an ADI CD of W_1 and a thickness of H, wherein the thickness of H is smaller than typical thickness as used in the prior art methods. The photoresist gate pattern 30 has a top surface 31 and vertical sidewalls 32. According to the preferred embodiment, the photoresist layer is commercially available positive-type photoresist. In another case, a bottom anti-reflection coating (BARC) may be interposed between the photoresist layer and the silicon nitride cap layer 18.

[0012] As shown in Fig.4, subsequently, a sputtered silicon thin film 50 is selectively coated on the top surface 31 and the vertical sidewalls 32 of the photoresist gate pattern 30. The exposed surface of the silicon nitride cap layer 18 that is not masked by the photoresist gate pattern 30 is substantially not sputtered with any silicon thin film. A selective silicon sputtering method is used to complete such selective silicon coating on the photoresist surface. The silicon thin film 50 has a thickness at the sidewalls 32

that is smaller than that at the top surface 31. As denoted, the thickness of the silicon thin film 50 on the sidewalls 32 is "x", while the thickness of the silicon thin film 50 on the top surface 31 is "y", wherein xx<. Preferably, x is less than 50 angstroms, more preferably, x is less than 10 angstroms.

[0013] As shown in Fig.5, using the sputtered silicon thin film 50 and the photoresist gate pattern 30 as etching hard mask, an anisotropic plasma dry etching is carried out to etch the silicon nitride cap layer 18. Since the sputtered silicon thin film 50 compensates the lateral etching in this etching step, there is substantially no CD loss when transferring the photoresist gate pattern 30 to the silicon nitride cap layer 18. The present invention features the use of sputtered silicon thin film 50 to protect the sidewalls 32 of the fine line photoresist gate pattern 30 when transferring the photoresist gate pattern 30 to the silicon nitride cap layer 18. The AEI CD of the gate pattern formed in the silicon nitride cap layer 18 transferred from the photoresist gate pattern 30 is W_1 that is substantially equal to the ADI CD of the photoresist gate pattern 30. Moreover, it is advantageous to use the present invention because the accuracy of pattern transferring may be improved. The

unexpected accuracy improvement results from that the photoresist gate pattern 30 is protected by the sputtered silicon thin film 50, and can be thus thinner, bringing out some benefits during lithographic process.

[0014] As shown in Fig.6, gate pattern is transferred to the silicon nitride cap layer 18. The sputtered silicon thin film 50 and the photoresist gate pattern 30 are consumed. The dry etching continues, using the patterned silicon nitride cap layer 18 as a hard mask, the tungsten silicide layer 16 and the polysilicon layer 14 are etched to form a gate structure 80 having an AEI CD of W_1 that is substantially equal to the ADI CD of the photoresist gate pattern 30.

[0015] Those skilled in the art will readily observe that numerous modification and alterations of the device may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.